Semiconductors

AN10046

ISP1581/2/3 Frequently Asked Questions

Rev. 03 — 18 July 2005 Application note

Document information

Info	Content
Keywords	isp1581, isp1582, isp1583, faq, usb, universal serial bus
Abstract	This document is a compilation of Frequently Asked Questions (FAQs) on Philips high-speed and full-speed Universal Serial Bus Peripheral Controllers: the ISP1581, ISP1582 and ISP1583.

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Revision history

Rev	Date	Description
03	20050718	Third release. Added Question 2.15.
02	20050427	Second release. Added Question 2.12, Question 2.13 and Question 2.14. Updated Fig 10.
01	20050301	First release.

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1. General product information

1.1 What are the differences between the ISP1581, ISP1582 and ISP1583?

The ISP1581/2/3 are cost-optimized and feature-optimized Hi-Speed Universal Serial Bus (USB) Peripheral Controllers. They fully comply with *Universal Serial Bus Specification Rev. 2.0*; supporting data transfer at high-speed (480 Mbit/s) and full-speed (12 Mbit/s).

Table 1: lists the major differences between the ISP1581, ISP1582 and ISP1583.

Table 1: Characteristic differences between the ISP1581, ISP1582 and ISP1583

Characteristic	ISP1581	ISP1582	ISP1583
Bus configuration	Generic and split bus	Generic	Generic and split bus
ATA/ATAPI interface	Yes	No	Yes
Power supply	5 V or 3.3 V (internal regulator)	3.3 V (no internal regulator)	3.3 V (no internal regulator)
I/O voltage	5 V or 3.3 V (internal regulator)	3.3 V	1.65 V to 3.6 V
Operating current	130 mA (high-speed)	45 mA (high-speed) 17 mA (full-speed)	47 mA (high-speed) 19 mA (full-speed)
Suspend current	450 µA (typical)	160 µA (typical)	160 µA (typical)
PIO RD/WR cycle time	80 ns	50 ns	50 ns
DMA slave RD/WR cycle time	78 ns	75 ns	75 ns
V_{BUS} sensing support	No	Yes	Yes
Package	LQFP64	HVQFN56	HVQFN64

2. Interfacing

2.1 Why should the IN endpoint buffer be properly cleared in the ISP1582/3?

If the USB connector is suddenly disconnected in the midst of a data transfer, there may be residual data in the IN endpoint buffer. This may cause data corruption during the next data transfer. To avoid data corruption, the IN endpoint buffer must be properly cleared.

For details on clearing the IN endpoint buffer, refer to *ISP1582/83 Clearing an IN Buffer (AN10045)* application note.

2.2 What is the fastest transfer speed achievable on the ISP1582/3?

For back-to-back data access, for both read and write, maintain a minimum cycle time of 50 ns (see Fig 1).

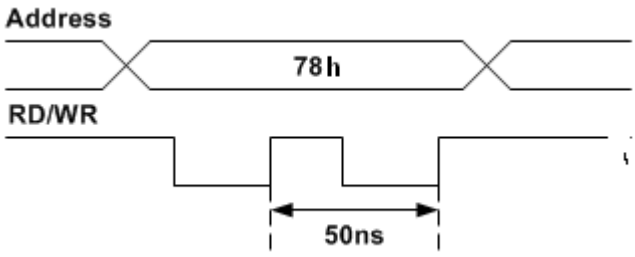

Fig 1. Back-to-back data access.

If the access is from write to read-or-write data on a different address, then the access time should be at least 91 ns. This also applies for read-or-write data to write access.

Fig 2 shows the read-to-read access of the Scratch register and the Chip ID register.

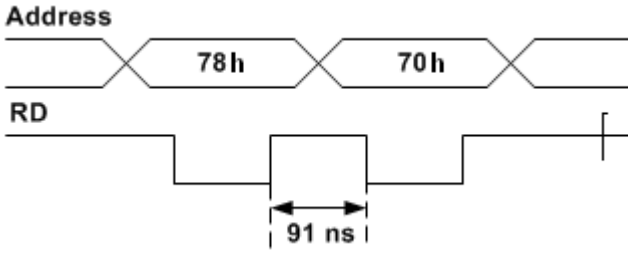

Fig 2. Read-to-read access of various addresses.

Fig 3 shows the write-to-write access to the Address register and the Interrupt Configuration register.

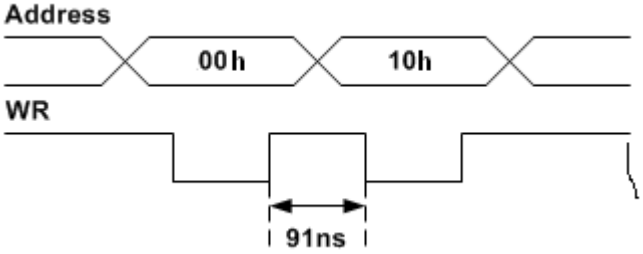

Fig 3. Write-to-write access of various addresses.

Fig 4 shows the write-to-read access of the Interrupt Configuration register and the Chip ID register.

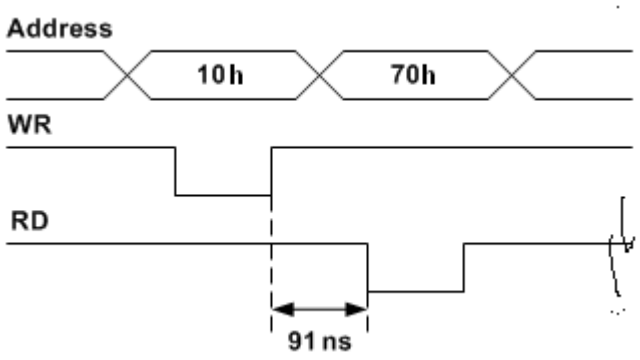

Fig 4. Write-to-read access of various registers.

Fig 5 shows the read-to-write access on the Chip ID register and the Interrupt Configuration register.

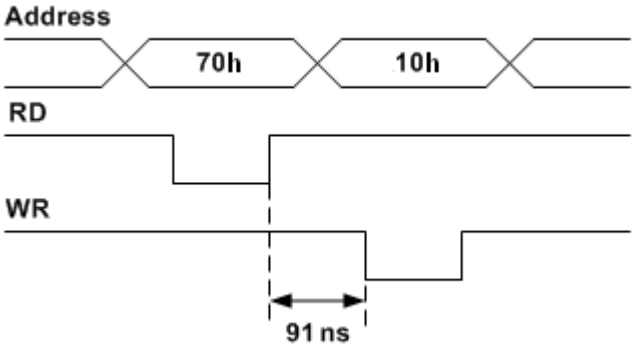

Fig 5. Read-to-write access of various registers.

2.3 When should the Buffer Length register and the Validate bit be used?

The Buffer Length register is used when the number of bytes is predetermined and buffer length validation is not required. It is useful when operating in generic processor mode, 16-bit data and 8-bit address, for an odd number of bytes. When an OUT token with zero-length packet is received, the Buffer Length register will reflect zero.

The Validate bit is used when the number of bytes to be sent to the IN endpoint is not predetermined. It is only used for an even number of bytes, when operating in generic processor mode. There is no restriction when in split bus mode.

Do not use the Buffer Length register together with the Validate bit because this will result in error.

2.4 What should be done if a suspend interrupt occurs along with a resume interrupt?

If a suspend interrupt occurs along with a resume interrupt, clear both the suspend the and resume interrupts. Do not service them.

Table 2: lists the conditions to service suspend and resume interrupts.

Table 2: Conditions to service the suspend and resume interrupts

Suspend	Resume	Action
0	1	Clear resume. Service resume.
1	0	Clear suspend. Service suspend.
1	1	Clear both suspend and resume. Do not service them.

2.5 Should control endpoints be also initialized when initializing other endpoints?

No. Control endpoints are self-initialized and are fixed at 64 B. Do not initialize control endpoints. Initializing control endpoints will result in errors.

2.6 Why is a transistor or MOSFET circuit needed on the V_{BUS} pin of the ISP1581?

The circuit is needed for the USB Compliance check. For a self-powered system, the Back-Voltage Test in the USB Compliance checks the voltage of V_{BUS}, DP and DM with respect to the ground, when the device is unplugged from a host or the host is suspended. The requirement for the Back-Voltage Test is that the voltage must not exceed 400 mV, after the device is unplugged or the host is suspended.

It is recommended that you have an external transistor or MOSFET to prevent back voltage on the DP and DM lines when the host is suspended or when the USB cable is disconnected. This is because the ISP1581 does not have any built-in V_{BUS} sensing. With the transistor or MOSFET acting as a V_{BUS} sensing, you can leave SoftConnect permanently on, and the transistor will handle the supply of 3.3 V to RPU with respect to the V_{BUS} presence.

Fig 6 shows the transistor or MOSFET circuit as well as the block diagram of the SoftConnect portion of the ISP1581.

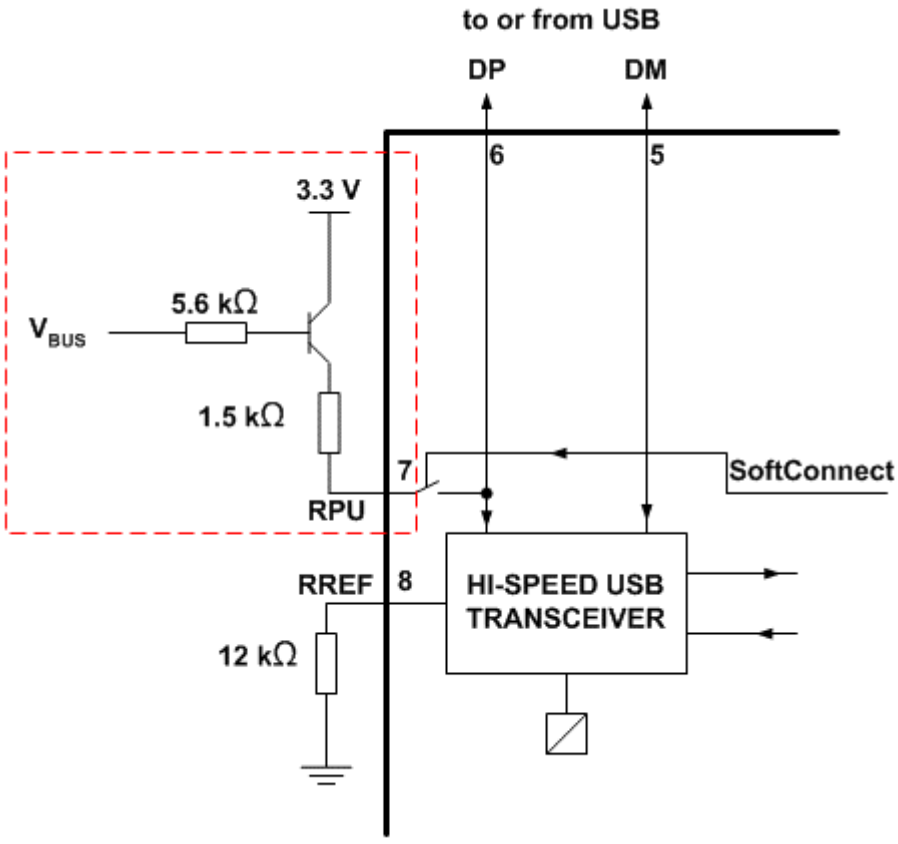

Fig 6. Transistor or MOSFET circuit.

2.7 Is it possible for the microcontroller to enable SoftConnect, when V_{BUS} is not present?

This is not advisable because it will cause a failure of the Back Voltage Compliance Test. SoftConnect should be enabled on detecting the presence of V_{BUS}.

For details, see Table 3:.

Table 3: Status of the chip

V_{BUS}	SoftConnect	Comments
Present	On Pull-up resistor on DP	Back voltage is not measured because enumeration process will begin
Not present	Off Pull-up resistor on DP is removed; suspend interrupt after 3 ms of no bus activity	Back voltage will be measured

2.8 In the Mode register of the ISP1582/3, how does the wake-up on chip select (WKUPCS) work?

The ISP1582/3 can be woken up using the wake-up on chip-select function. To use this function, the WKUPCS bit must be set to logic 1 before the ISP1582/3 enters suspend mode. To wake up the ISP1582/3, assert the chip select and perform a valid register

read. The reading of registers must be done within the ISP1582/3 address range. CS_N and RD_N must be asserted together for the ISP1582/3 to wake up from suspend mode.

Performing a valid register write is not recommended because registers may be locked from writing after the ISP1582/3 goes into suspend mode.

2.9 In the ISP1582/3, how long does it take for V_{BUS} to charge and discharge?

It takes V_{BUS} about 22 ms to charge and 1.8 sec to discharge. This measurement is done using a 10 kΩ series resistor, in addition to 1 MΩ and 1 µF on V_{BUS}.

It is recommended that you connect a 10 kΩ-to-200 kΩ series resistor on V_{BUS} as an additional protection for the V_{BUS} pad.

Fig 7 shows the connection diagram for V_{BUS}.

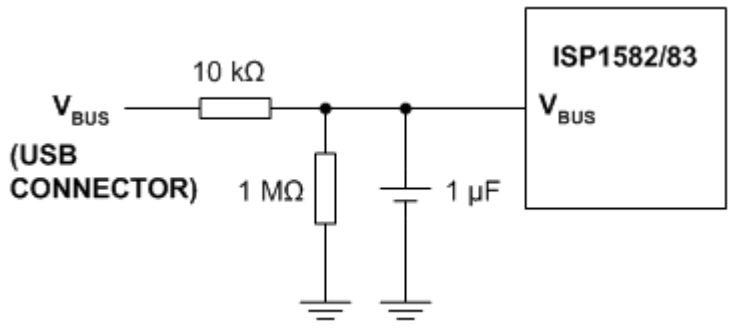

Fig 7. V_{BUS} connection diagram.

Fig 8 shows the waveform for the charging of V_{BUS}.

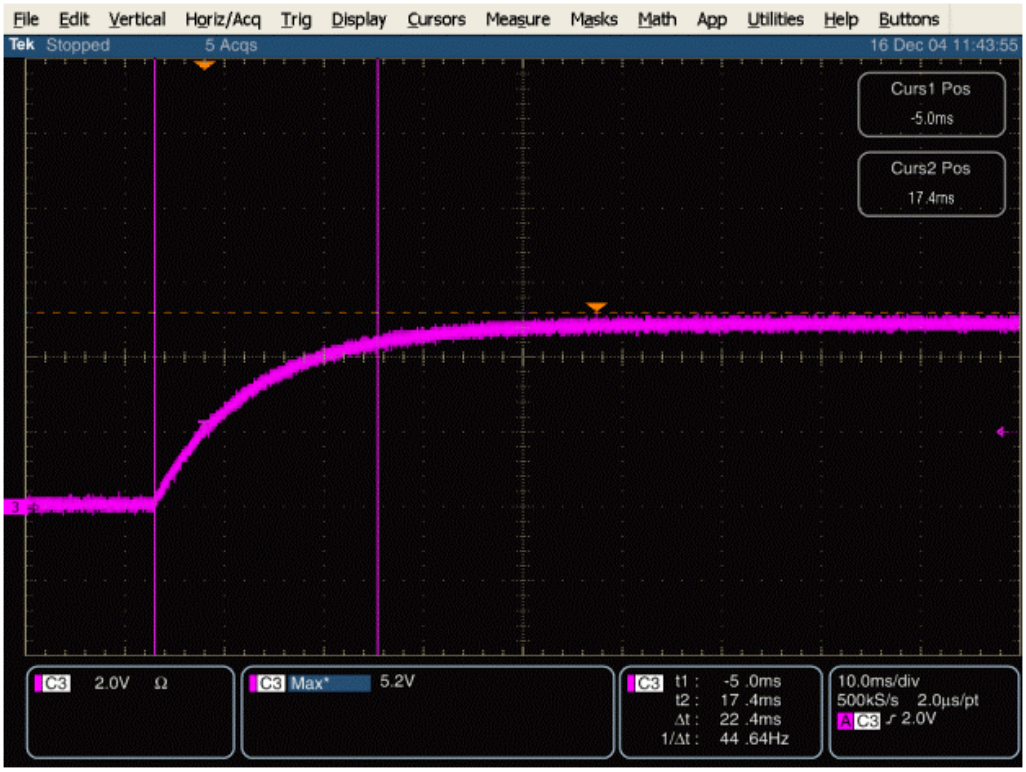

Fig 8. V_{BUS} charging waveform.

Fig 9 shows the waveform for the discharging of V_{BUS}.

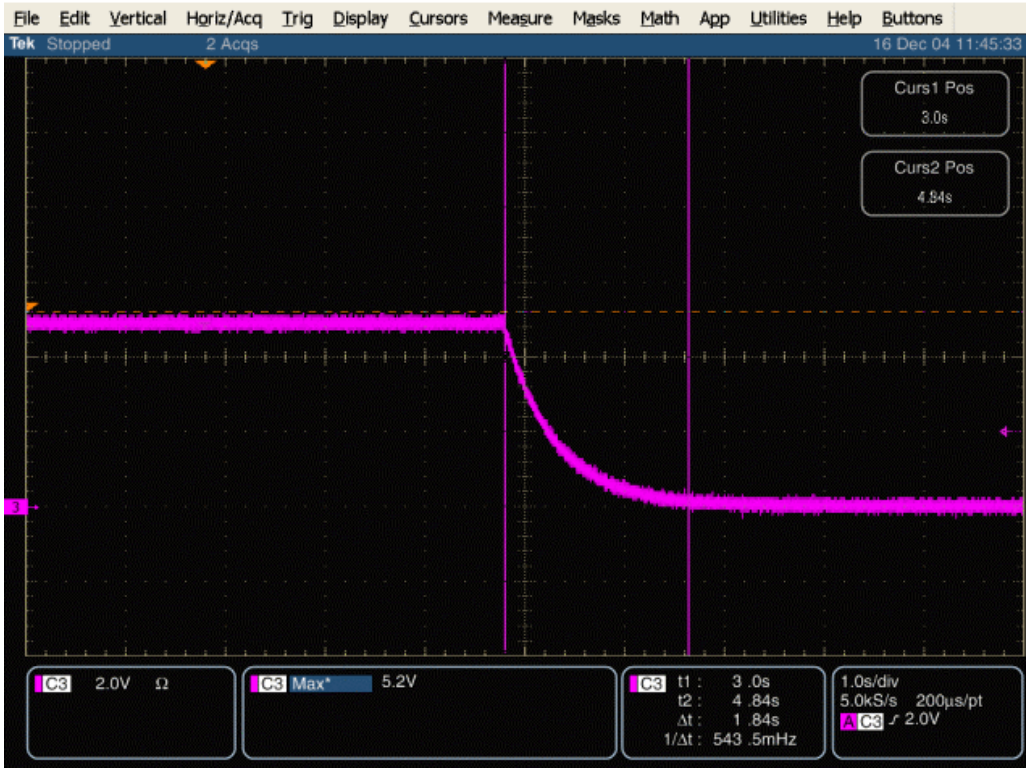

Fig 9. V_{BUS} discharging waveform.

2.10 How to configure the ISP1583 in GDMA master mode?

Perform the following settings to configure the ISP1583 DMA as a master in non-ATA mode:

- DMA Configuration register (38h): the ATA_MODE bit is set to logic 1 → configures the DMA for MDMA mode.
- DMA Hardware register (3Ch), the MASTER bit is set to logic 1 → the ISP1583 is configured in Generic DMA (GDMA) master mode.

When you are using the ISP1583 as DMA master, DREQ will act as an input pin, and DACK, DIOR and DIOW will act as output pins. The DREQ signal must be asserted (active HIGH by default) for any DMA activities. If no activity is seen after asserting DREQ, ensure that the EOT pin is not asserted.

2.11 In the ISP1583, how to interface to the ColdFire processor using the Generic Processor mode in the ISP1582 and Split Bus mode?

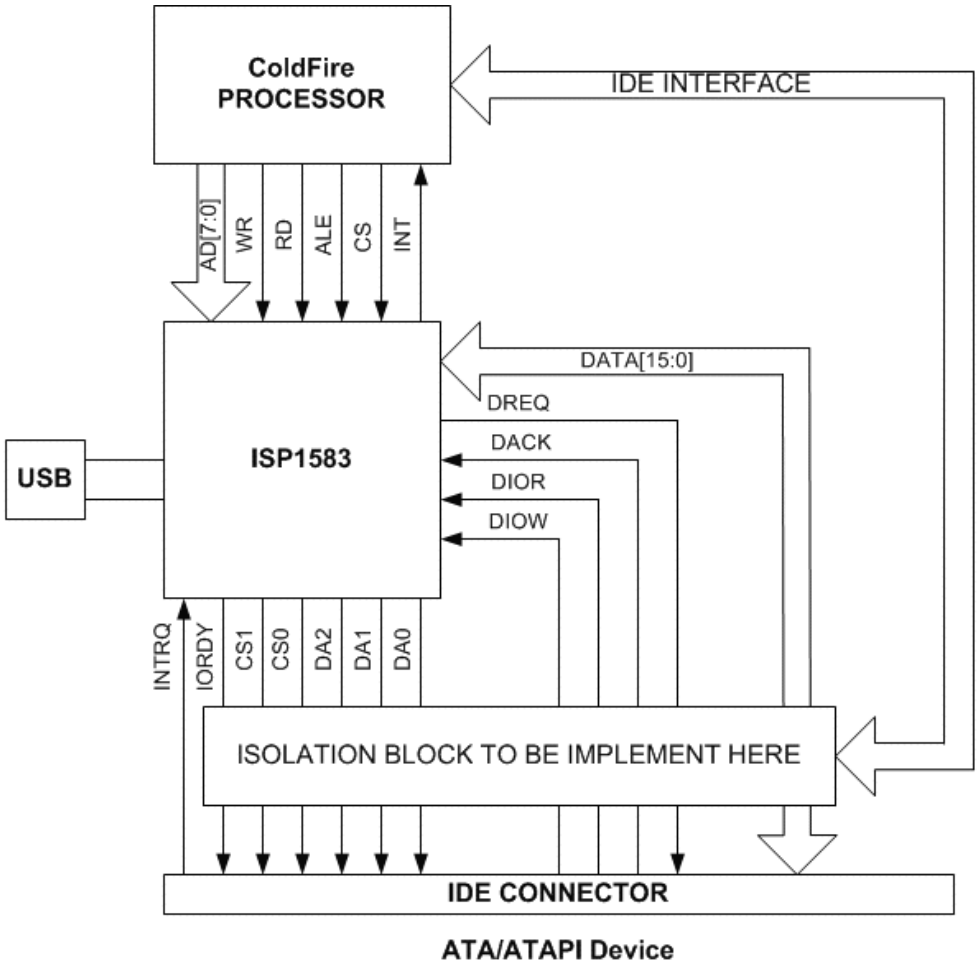

Fig 10. Example for interfacing the ISP1583 MP3 application in split bus mode.

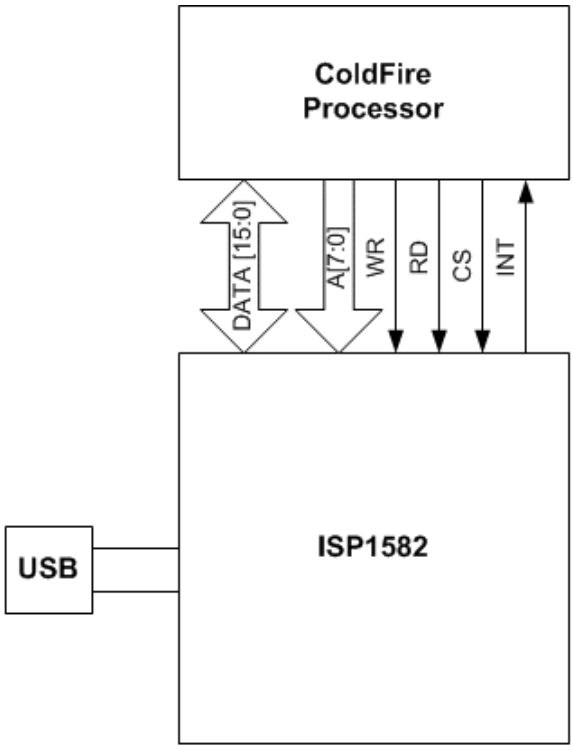

Fig 11. Example for interfacing the ISP1582 MP3 application in generic processor mode.

Remark: Question 2.12, Question 2.13 and Question 2.14 are related to Philips application note *Interfacing the ISP1582 to the Intel PXA250 Processor (AN10038)*. For details, refer to the application note.

2.12 Why must an OR operation be performed between ADDR24 and ADDR25 for CS_N?

An OR operation must be performed between ADDR24 and ADDR25 in generic processor mode to determine whether it is a PIO or DMA range, that is, a PIO transfer or a DMA transfer.

PIO transfer: CS_N will be asserted for PIO transfer; see Fig 12.

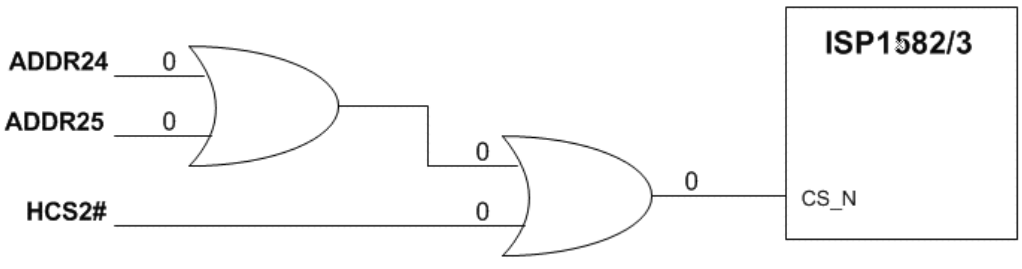

Fig 12. PIO transfer in generic processor mode example.

DMA transfer: CS_N will be deasserted for DMA transfer; see Fig 13. For DMA mode, CS_N is not needed and should be masked off.

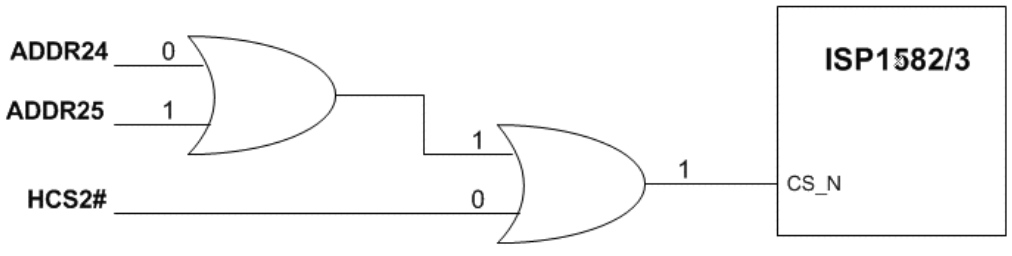

Fig 13. DMA transfer in generic processor mode example.

PIO or DMA transfer: If you are using the following address range, then you can just OR ADDR25 and HCS2# because ADDR24 is always 0; see Fig 14. If, however, you are using a different address range, then Fig 12 and Fig 13 must be implemented, that is, OR ADDR24 and ADDR25.

- PIO address range: 0000 0000h to 00FF FFFFh
- DMA address range: 0200 0000h to 02FF FFFFh.

Fig 14. PIO or DMA transfer in generic processor mode example.

2.13 Why must an OR operation be performed between ADDR25 and CS_N for DACK?

DMA transfer: ADDR25 is needed for the DACK pin because the DACK signal is needed when performing DMA. XScale provides the DACK signal through a logic process.

- PIO address range: 0000 0000h to 00FF FFFFh
- DMA address range: 0200 0000h to 02FF FFFFh

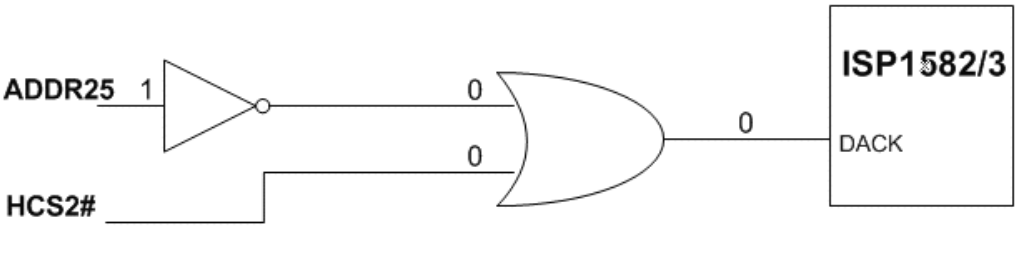

Fig 15. DMA transfer in generic processor mode example.

In Fig 15, if ADDR25 is set to 1, it will become 0 after going through the inverter. Both the outputs—inverter and HCS2#—will go through the OR gate and output as 0. DACK in the ISP1582/3 is active LOW by default and so DACK is set.

2.14 Why must A[9:2]of PXA250 be connected to A[7:0] of the ISP1582/3?

The ISP1582/3 is a 16-bit data bus. When you connect A[9:2] of PXA250 to A[7:0] of the ISP1582/3, the word alignment is perfect because the processor is 32 bits and there is no performance problem.

2.15 In the ISP1582/3, what is the minimum time required for the Buffer Status register to get updated?

In the ISP1582/3, when you try to consecutively send a few USB data packets, with double buffering enabled and you are using the Buffer Status register (address 1Eh) to determine if there are any buffers available for more packets, the firmware must allow at least 200 ns delay between the writing of the data packet and the reading of the Buffer Status register. If the firmware issues a Read Buffer Status register after the write command in less than 200 ns, the firmware will read an incorrect buffer status; see Fig 16. The firmware will then start to refill buffers assuming that the buffers are already emptied, overwriting unsent data in the buffer.

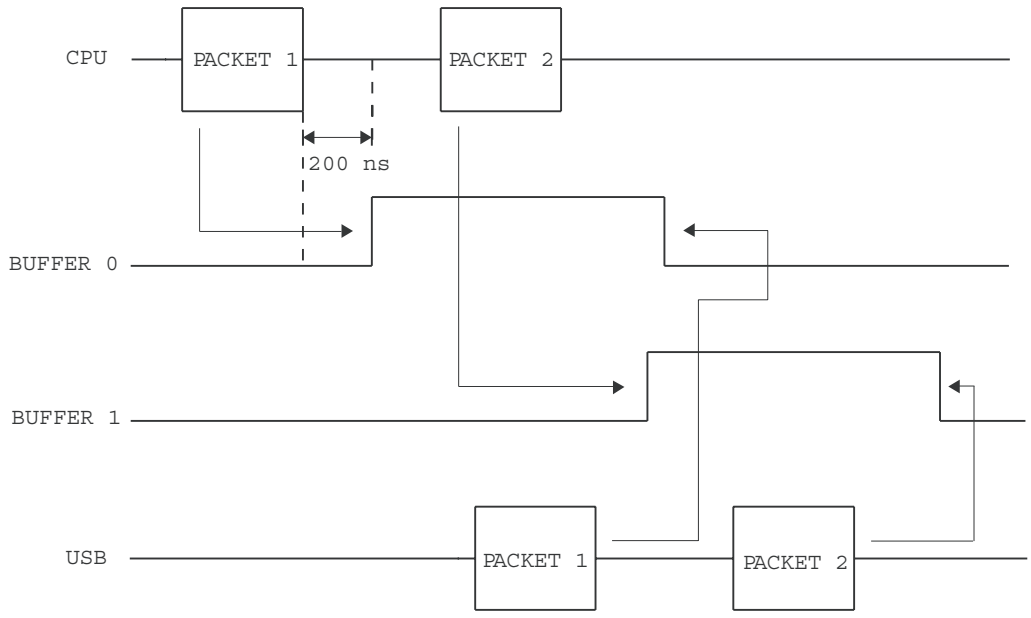

Fig 16. 200 ns delay between reading and writing of data in the Buffer Status register.

3. Clocking

3.1 What should be the voltage swing if an external clock is used on the ISP1582 or ISP1583?

For the ISP1582/3, the voltage swing for the external clock should be 1.8 V. The ISP1582/3 will not function if 3.3 V is supplied. Fig 17 shows the capacitor circuit that can successfully lower the swing from 3.3 V down to 1.8 V.

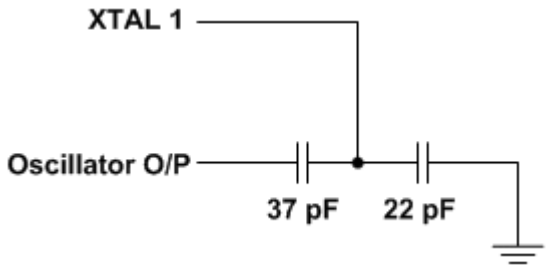

Fig 17. Capacitor circuit to lower the swing from 3.3 V to 1.8 V.

Fig 18 shows the input swing of 3.3 V using a function generator.

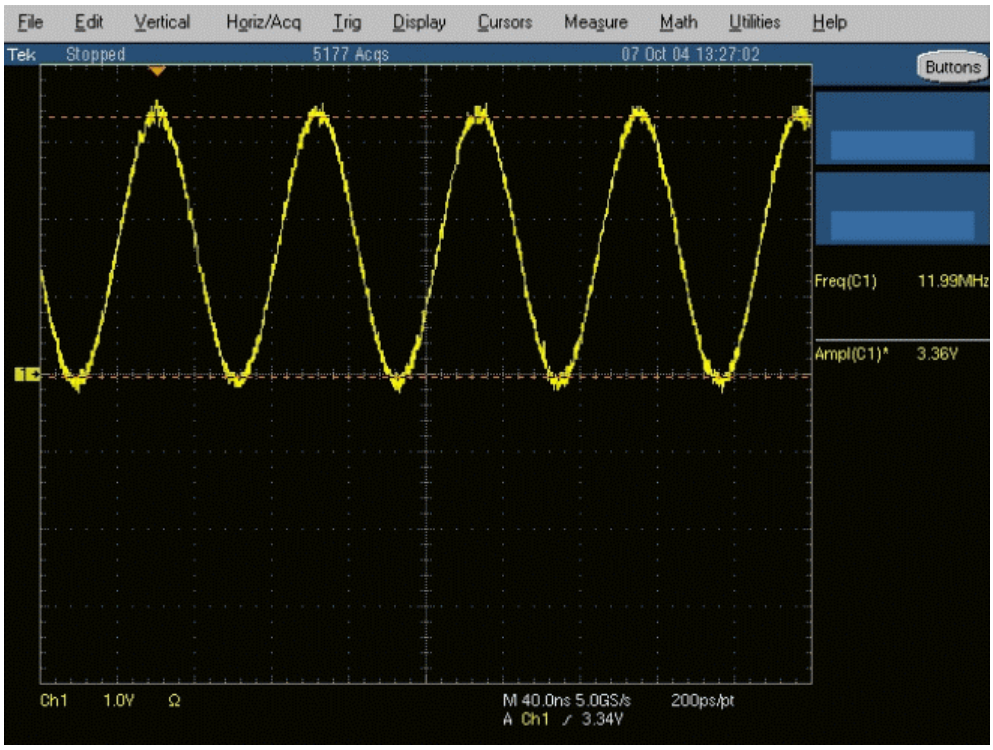

Fig 18. Input swing of 3.3 V, before adding the capacitance circuit.

Fig 19 shows that the 3.3 V swing is lowered to 1.8 V after the capacitance circuit is added.

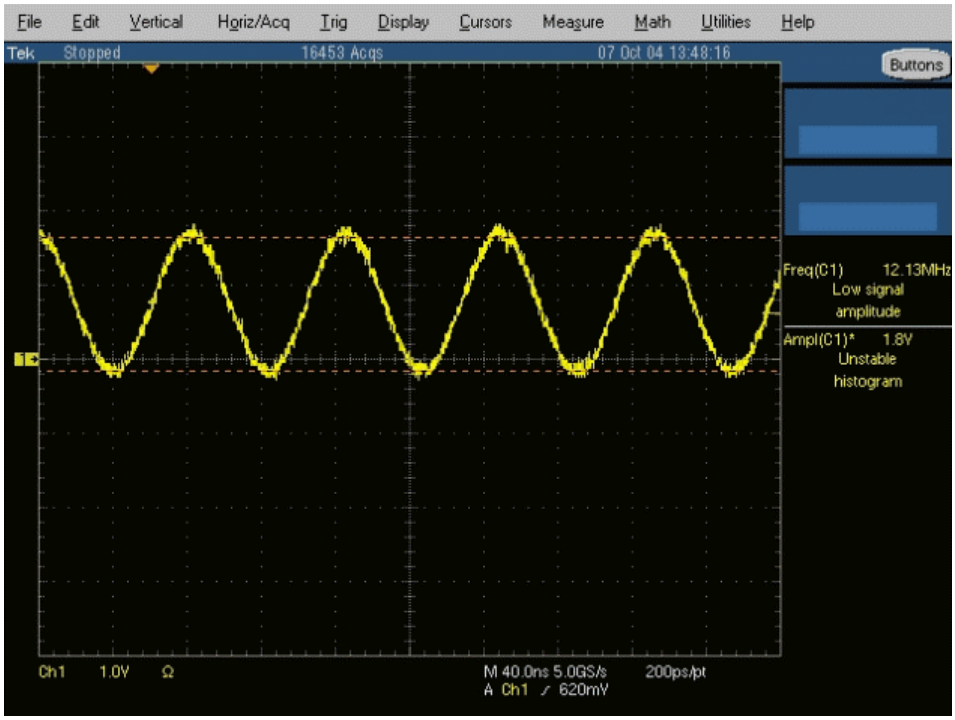

Fig 19. Input swing is reduced to 1.8 V, after adding capacitance circuit.

3.2 How long does it take for the clock to stabilize if the ISP1582/3 wakes up on chip select?

As tested, it takes about 600 ns for the clock to stabilize if the ISP1582/3 wakes up on chip select. This timing, however, may not be sufficient for the chip. This is because the internal oscillator will take more than 500 µs to start up while the Phase-Locked Loop (PLL) takes another 500 µs to start up. It is, therefore, recommended that you wait for a minimum of 2 ms before performing a write or read operation.

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